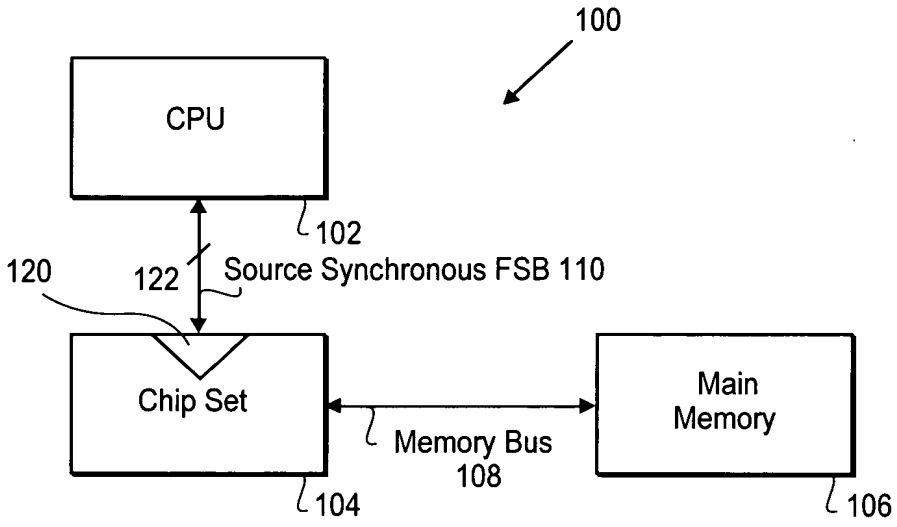
100
CPU
102
120
122
Source Synchronous FSB 110
Chip Set
Memory Bus
108
Main
Memory
104
106

FIG. 1

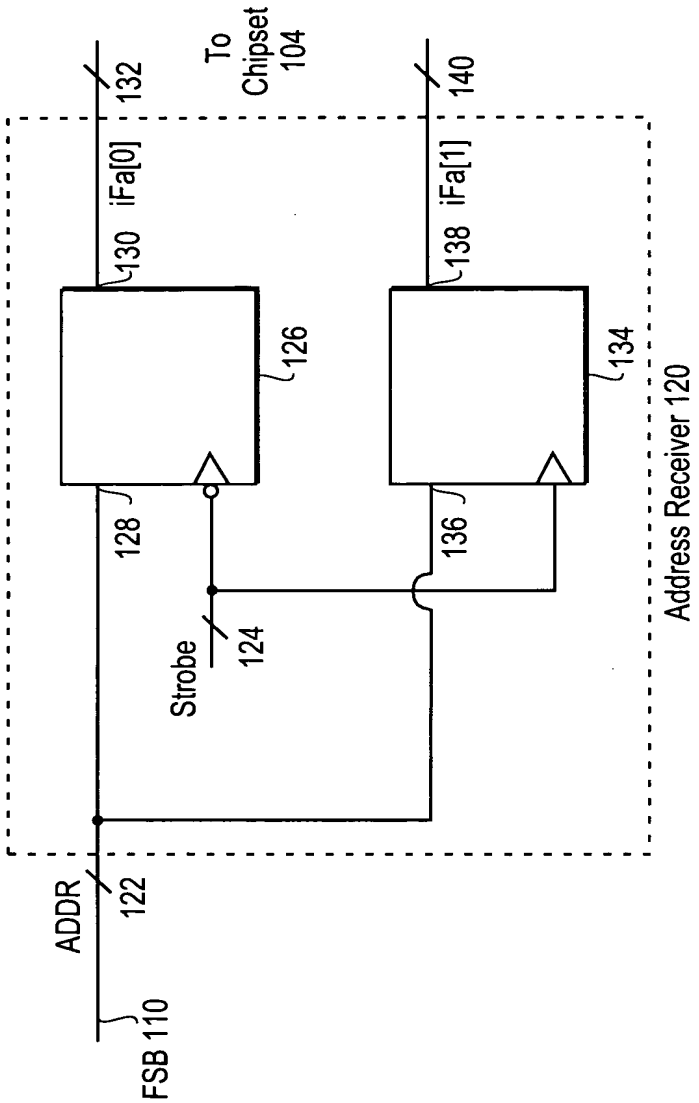
To Chipset 104
132
140
iFa[0]
iFa[1]
130
138
126
134
128
136
Strobe
124
Address Receiver 120
ADDR
122
FSB 110

FIG. 2

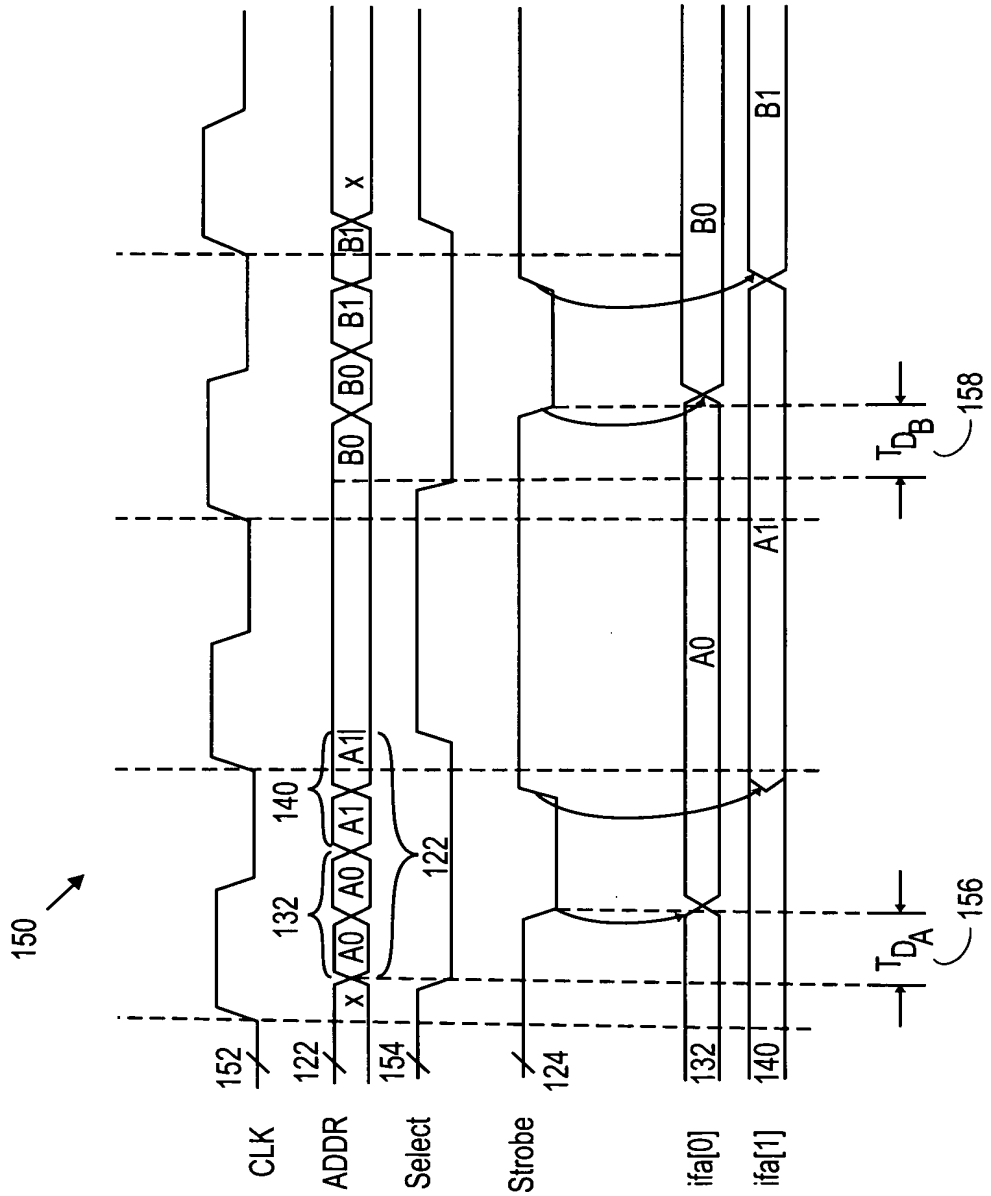
150
CLK
ADDR
Select
Strobe
ifa[0]
ifa[1]
152
122
154
124
132
140
x
A0
A1
B0
B1
122
T_{D_A}
156
T_{D_B}
158

FIG. 3

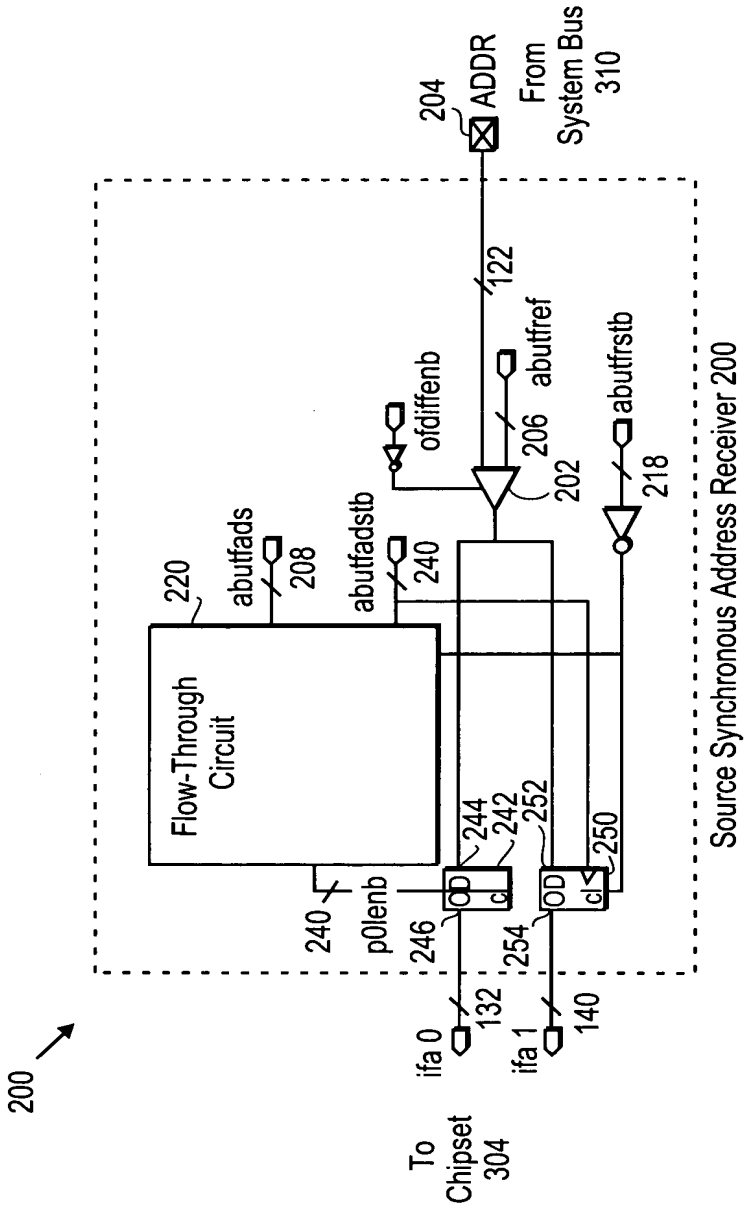
200
204
ADDR
From System Bus 310
122
ofdiffenb
abutfref
206
202
abutfrstb
218
abutfads
208
abutfadstb
240
220
Flow-Through Circuit
Source Synchronous Address Receiver 200
244
242
252
250
OD
CL
240
p0lenb
246
254
132
140
ifa 0
ifa 1
To Chipset 304

FIG. 4

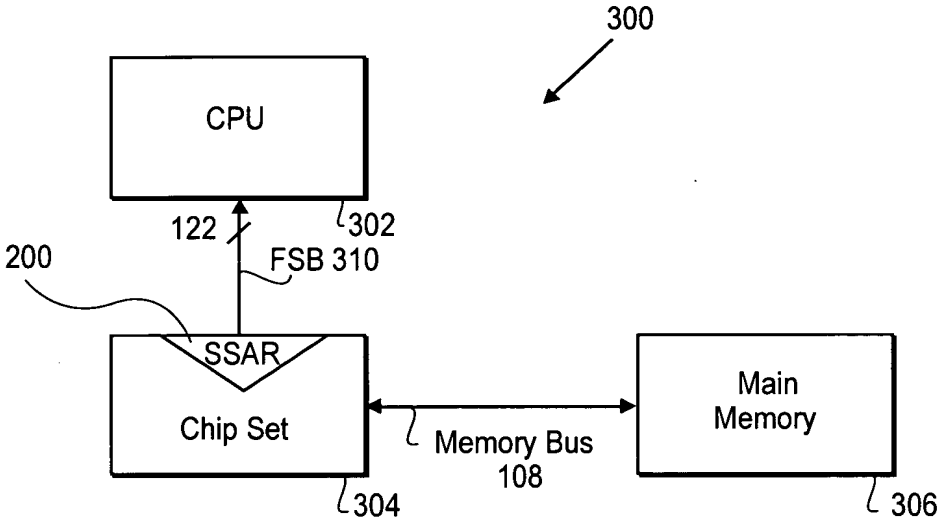
300
CPU
122
302
200
FSB 310
SSAR
Chip Set
Memory Bus
108
Main
Memory
304
306

FIG. 5

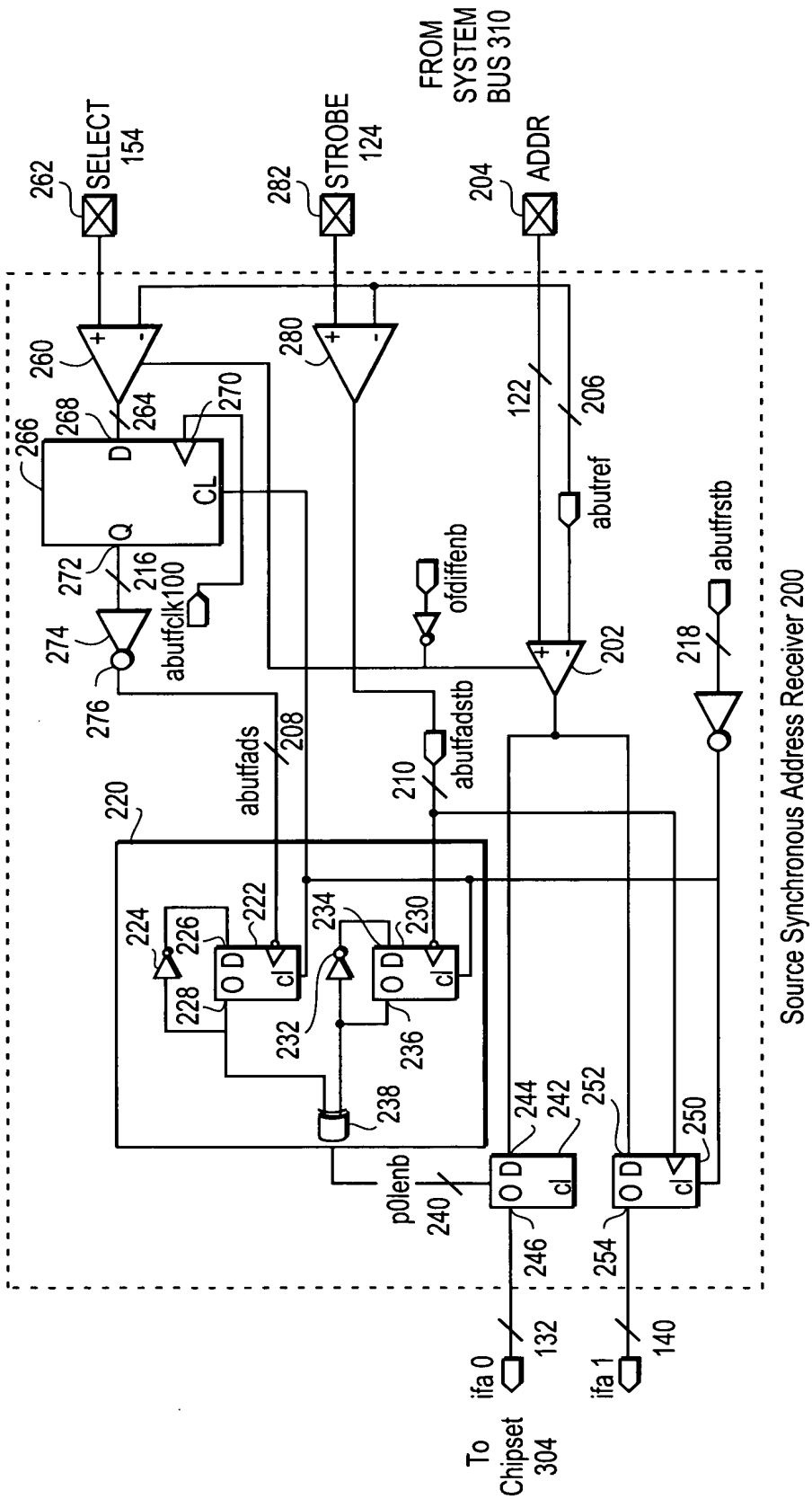
FROM SYSTEM BUS 310
SELECT 154
STROBE 124
ADDR
262
282
204
260
280
122
206
266
268
264
270
D
CL
Q
272
216
abutfclk100
abutref
ofdiffenb
abutfrstb
274
276
202
218
abutfads
208
abutfadstb
210
220
224
226
222
234
230
228
232
236
238
O D
cl
244
242
252
250
p0lenb
240
246
254
ifa 0
132
ifa 1
140
To Chipset 304
Source Synchronous Address Receiver 200

FIG. 6

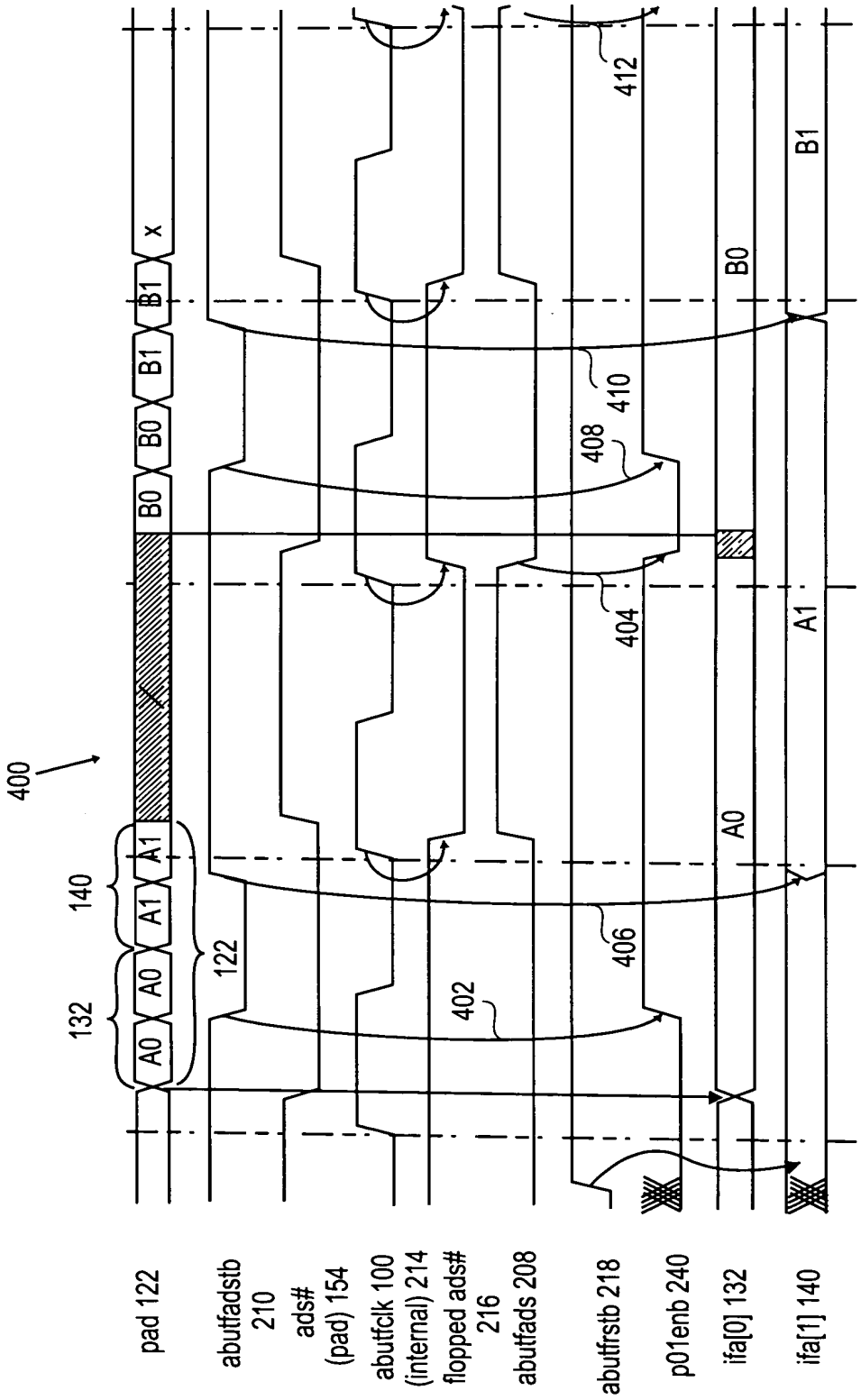
400
132
140
122
A0
A0
A1
A1
B0
B0
B1
B1
x
402
404
406
408
410
412
A0
A1
B0
B1
pad 122
abutfadstb 210
ads# (pad) 154
abutfclk 100
(internal) 214
flopped ads# 216
abutfads 208
abutfrstb 218
p01enb 240
ifa[0] 132
ifa[1] 140

FIG. 7